IN THE CLAIMS:

1. (Previously Presented A plasma display panel comprising:

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode pair comprising a sustain electrode and a bus electrode,

a dielectric layer covering the display electrodes, and a protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a dielectric layer covering the address electrodes, and

linear ribs located between the address electrodes, with phosphor layers located on the ck plate between the adjacent linear ribs so that they each extend intermittently in the lengthwise direction of the ribs for each pixel wherein

(1) each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel,

(2) each pixel is formed by a crossing region of the address electrode and the display electrode pair, and

(3) each phosphor extends intermittently in the lengthwise direction of the ribs creating regions on the ribs and the dielectric layer that have no phosphor layer and that correspond to the regions between the adjacent display electrode pairs.

2. (Original) The plasma display panel as claimed in claim 1, further comprising linear shield layers on the front plate parallel to each other, wherein each shield layer is located between an adjacent display electrode pair to be parallel to the display electrode pairs.

3. (Previously Presented) A plasma display panel comprising:

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode comprising a sustain electrode and a bus electrode,

a dielectric layer covering the display electrodes, and a protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a light-absorbing layer covering the address electrodes, and

linear ribs located between the address electrodes, with phosphor layers located on the back plate between the adjacent linear ribs so that they each extend intermittently in the lengthwise direction of the ribs for each pixel, wherein

(1) each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel,

(2) each pixel is formed by a crossing region of the address electrode and the display electrode pair, and

(3) each phosphor extends intermittently in the lengthwise direction of the ribs creating regions on the ribs and the dielectric layer that have no phosphor layer and that correspond to the regions between the adjacent display electrode pairs.

4. (Original) The plasma display panel as claimed in claim 3, wherein the light-absorbing layer contains a dark pigment and a dielectric substance.

5. (Previously Presented) A plasma display panel comprising:

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode comprising a transparent sustain electrode and a non-transparent metal bus electrode,

a translucent dielectric layer covering the display electrodes, and a magnesium oxide-containing, translucent protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a dark dielectric layer covering the address electrodes,

linear ribs located between the address electrodes, and phosphor layers provided on the back plate between the adjacent linear ribs so that a red-emitting phosphor layer, a blue-emitting phosphor layer and a green-emitting phosphor layer adjacent each other with a rib therebetween and these three different phosphor layers each extend intermittently in the lengthwise direction of the ribs, wherein

(1) each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel,

(2) each pixel is formed by a crossing region of the address electrode and the display electrode pair, and

(3) each phosphor extends intermittently in the lengthwise direction of the ribs creating regions on the ribs and the dielectric layer that have no phosphor layer and that correspond to the regions between the adjacent display electrode pairs.

6. (Original) The plasma display panel as claimed in claim 5, further comprising linear shield layers on the front plate parallel to each other, wherein each shield layer is between the adjacent display electrode pairs and parallel to the display electrode pairs.

7. and 8. (Canceled)

9. (Previously Presented) A plasma display panel comprising:

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode pair comprising a sustain electrode and a bus electrode,

a dielectric layer covering the display electrodes, and a protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a dielectric layer covering the address electrodes, and

linear ribs located between the address electrodes, with a phosphor layer located on the back plate in each of a plurality of adjacent cell spaces formed by a plurality of adjacent linear ribs, said phosphor layers being intermittently interrupted creating regions on the ribs that have no phosphor layer and that corresponds to the regions between the adjacent display electrode pairs wherein

(1) each phosphor layer covers the surface of the dielectric layer and the surface of the linear ribs within each pixel, and

(2) each pixel is formed by a crossing region of the address electrode and the display electrode pair.

10. (Original) The plasma display panel as claimed in claim 9, further comprising shield layers in the regions between the adjacent and parallel to the display electrode pairs on the front plate.

11. (Original) The plasma display panel as claimed in claim 9, further comprising a dark layer on the entire surface of the back plate below the linear ribs and below the phosphor layers.

12. (Canceled)